# Adarsh Patil

## Contact information


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## Profile summary

I bring proven research experience at both target-oriented industry labs and blue-skies academic research. My research contributions and publications aim to holistically design next generation systems, specifically memory systems for various application domains and compute paradigms - HPC, AI, serverless. My ethos of application driven hardware research is reflected in all my works, each of which span several aspects of my proficiency

I possess effective technical communication skills and have consistently proven my ability to meet deadlines and achieve project objectives. I work well in a team as well as independently. I am a constant learner, striving to expand my sphere of understanding. My education and industry experience has helped me develop technical capabilities in several adjacent areas within computer systems - operating systems, compilers, JIT libraries, network interconnect, analytical and mathematical modeling.

## Education

**August 2023** — Doctor of Philosophy
University of Edinburgh, United Kingdom [ARM PhD Fellowship]
Thesis: Co-designing reliability and performance for datacenter memory
Advisor: Prof. Vijay Nagarajan

**July 2017** — M.Tech. (Research)
Indian Institute Of Science (IISc), Bangalore, India
Thesis: Heterogeneity Aware Shared DRAM Cache for Integrated Heterogeneous Architectures
GPA: 6.33/8.0 - magna cum laude
Advisor: Prof. R Govindarajan

**May 2012** — Bachelor of Engineering
Ramaiah Institute of Technology (RIT), Bangalore, India
GPA: 9.40/10.0 - summa cum laude

## Professional experience

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|---|---|
| Dec 2023 - Current | Senior Research Engineer at Arm, UK<br>Systems architecture & technology group |
| Apr 2023 - Nov 2023<br>(8 months) | Postdoctoral Research Associate at University of Edinburgh, UK<br>Algorithms for next generation cloud systems |
| Aug 2017 - Apr 2019<br>(1 year 8 months) | Research Scientist at Intel Corporation, Bangalore, India<br>HPC Ecosystem and Applications Team |
| Jun 2012 - Jul 2014<br>(2 years 1 month) | Technology Analyst at Goldman Sachs, Bangalore, India<br>Core Platform Engineering |
| Jun 2011 - Aug 2011 | Summer Analyst at Goldman Sachs, Bangalore, India<br>Automation workflows for datacenter resource provisioning and error triage |

## Referred research publications

| | |
|---|---|
| HCDS @ ASPLOS 2024 | UDON: A case for offloading to general purpose compute on CXL memory https://adar.sh/apta |
| DSN 2023 | $\bar{A}$pta: Fault-tolerant object-granular CXL disaggregated memory for accelerating FaaS https://adar.sh/apta |
| ISCA 2021 | Dvé: Improving DRAM Reliability and Performance On-Demand via Coherent Replication https://adar.sh/dve |
| TACO 2017<br>Best Poster EECS 2017, Presented HiPEAC 2018 | HAShCache: Heterogeneity-Aware Shared DRAMCache for Integrated Heterogeneous CPU-GPU Systems https://adar.sh/hashcache-taco |
| Arm / UEd Conference 2021 | Improving Reliability and Performance of Datacenter Systems via Coherence https://adar.sh/arm-ed-conf-2021 |
| UK Systems 2021 | FaaS with CXL Disaggregated Shared Memory |

## Projects

**Projects at Univ of Edinburgh**

Redesigning datacenter co-ordination services for next generation hardware
- Novel hardware primitives for disaggregated memory
- Employing new algorithms for synchronization and scheduling

Achieving persistence through replicated disaggregated memory

**Projects at Intel**

Research into high-performance software, hardware, and systems for AI
- Optimized compute libraries for neural networks - libxsmm, MKL-DNN
- Architecture specific parallel algorithms - register blocking, vectorization
- Datatypes for matrix representation - low-precision, sparsity
- Hardware architecture design proposals with a deep understanding of underlying algorithms

**Projects at Indian Institute of Science**

Address translation overheads in next generation x86 processors
- TLB and Pagewalk performance in multicore architectures with large Die-Stacked DRAM Cache [Tech Report 2015, arXiv]
  https://adar.sh/caffe-compiler-optimize

Program flow prediction in mobile devices
- Accuracy of hardware branch predictor in ARM processors running Android
  https://adar.sh/BranchPredAndroid

Compiler optimization transforms to improve performance on CPUs
- Harris Corner Detection: https://adar.sh/compiler-optimize
- Caffe Neural Networks: https://adar.sh/caffe-compiler-optimize

Dynamic Scoping for C Language in Clang compiler https://adar.sh/VarMutate

Database query optimization: Selectivity estimation of predicates in queries
- ESS Dimensions Reduction for Plan Bouquet https://adar.sh/PlanIkebana

**Projects at Goldman Sachs**

Architect, design and implement solutions of various virtualization & linux technologies spanning datacenter compute, storage, networking

Hardware and OS Performance Benchmarking & Analysis

- Authored an automated benchmarking framework to run and report performance by running test suites on VMs and Baremetals
- Performance analysis & tuning for specialized internal apps ( e.g. low Latency, high I/O, memory, network intensive )
- Test Suites – SpecJBB, kmake, blacksholes, Dhrystone, Whetstone, Hackbench, Disk tests, Network uperf, lat proc

Linux Containers

- Architecting and implementing Containers for Goldman Sachs Cloud
- Possess a good understanding of underlying technology Namespaces, Cgroups, SELinux, Network configuration, Libvirt API

Thin client desktop VDI solution

- Engineered a Minimized and locked down Linux based solution
- Authored several PyGTK and X11 based applications for remote management, diagnostics, troubleshooting and NEA
- Network booted, kickstart and preseed based unsupervised install
- Engineered a stateless RAM-based network booted system on ARM based hardware

Engineering Nested Virtualization (Bromium vSentry) as a security solution

Vendor Interaction and liaising – Intel, VMware, Redhat

**Projects at M S Ramaiah Inst of Tech**

Spoken language identification using machine learning
[Bachelor's dissertation] https://adar.sh/spokenlang

SNIDS: An Intelligent & Multiclass Support Vector Machines Based NIDS
[ICECIT 2012] https://adar.sh/S-NIDS
funded by Defense Research and Development Organization (DRDO), India

Line Birds (game) using OpenGL https://adar.sh/linebird
A parallel algorithm for Max Flow Algorithm using Ford-Fulkerson method
Lead developer of a student focused Linux Distro "ANDROMEDA Linux"

## Achievements and awards

- Founding trustee of Dr. M R Gorbal Foundation - a charitable organization which aims to promote research in Physics (2022)
- Best Poster at Electrical Science Divisional Symposium at IISc (2017)
- Certificate of distinction - Data Science Course, Johns Hopkins University on Coursera (2014)
- Best outgoing achiever - Dept. of CSE at RIT, (2012)
- First Place at National Level Project Competition held at RIT (2012)
- Second Place at "Random Hacks of Kindness #2" hackathon (2010)

## Professional Activies

- ACM SIGARCH content editor, March 2024 - Present
- Web chair HPCA 2024
- Informatics Science Communication Group, Dec 2021 - Nov 2023
- ICSA@Informatics social media communication, Sept 2021 - Nov 2023
- Teaching assistant/Tutor INF2C-CS, University of Edinburgh, Aug 2019 - Dec 2019
- Student System Admin at CSA Department, IISc, Aug 2014 - Dec 2016
- Teaching Associate for the CUDA Teaching Centre, RIT, Jan 2012 - May 2012
- Chairman of VRGLINUG (GNU/Linux users group at RIT),
  Secretary and member of executive committee of IEEE, RIT
  Influential Member of RoboMSR, CodeMSRIT, Assoc. of Computer Engineers, 2011-12

## Miscellaneous

**Strengths**

- Adaptability, Quick learner, Hardworking and Dedication
- Effective communicator and good leadership skills
- Always updated with latest technology and trends of market.
- Analytical and mathematical problem solving ability

**Hobbies**

- Avid endurance athlete: 2 full and 18 half marathons, stadium runs, 100K cycle
- Hiking enthusiast - 5 Munros, several Corbetts, coastal and trail walks
- Blogging and research communication
- Organizer: HPCA 2024, TEDx, Pycon India, Random Hacks of Kindness

**Other Links**

github.com/adarshpatil
in.linkedin.com/in/adarshpatil

**References**

Academic References
Vijay Nagarajan, PhD Advisor
Professor, University of Edinburgh / University of Utah
vijay.nagarajan@ed.ac.uk, vijay@cs.utah.edu

Prof. R Govindarajan, Master's Advisor
Professor, IISc
govind@serc.iisc.ernet.in

Industry References
Bharat Kaul
Director, Intel Parallel Computing Lab

## Keywords

✓Academic research (PhD) ✓Industrial research experience ✓Memory architecture ✓System design ✓Architectural modeling and simulation ✓Reliability, availability and serviceability (RAS) ✓Coherence protocols ✓CXL, OpenCAPI ✓Disaggregated memory ✓Serverless computing ✓CPU, GPU, SoC architecture ✓DRAM, HBM, HMC, DDR memory